REMARKS

In the present Office Action, the title is objected to as not descriptive of the invention to which the claims are directed. In response, Applicant has proposed a new title in accordance with the Examiner's recommendation. Applicant therefore respectfully submits that the objection to the title is overcome.

Next, the drawings are objected to under 37 C.F.R. § 1.83(a) for failing to illustrate calculating a speculative target memory address utilizing contents of at least one register without regard for whether the register contents will be modified. In response, Applicant has proposed new Figure 4, which is a flowchart including a block 112 that explicitly recites that the target address of the prefetch operation (e.g., PRE) is calculated without regard as to whether a register value utilized in the target address calculation will subsequently be modified prior to execution of a corresponding load operation. Support for proposed Figure 4 may be found in Table I at page 11 of the present specification and the corresponding description at page 11, line 13 through page 14, line 10. Because proposed Figure 4 and the corresponding description proposed herein are entirely supported by the specification as originally filed, Applicant submits that Figure 4 does not contain any new matter and the proposed amendments to the written description and drawings should be entered.

Applicant notes with appreciation the Examiner's indication in paragraph 5 of the present Office Action that the rejection in view of *Eickemeyer* is withdrawn.

In paragraph 7 of the present Office Action, Claim 18 is rejected under 35 U.S.C. § 112, second paragraph, as lacking antecedent basis for the recitation "said plurality of registers." The deletion of this phrase from Claim 18 in the present Amendment overcomes this rejection.

Next, in paragraph 9, Claims 17-19, 23-25 and 29 are rejected under 35 U.S.C. § 102(b) as anticipated by Chen and Baer, "Effective Hardware-Based Data Prefetching for High-Performance Processors," IEEE Transactions on Computers, Vol. 44, No. 5, 1995 (hereinafter *Chen*). In addition, Claims 20 and 26 are rejected under 35 U.S.C. § 103(a) as unpatentable over

Chen, Claims 21 and 27 are rejected under 35 U.S.C. § 103(a) as unpatentable over *Chen* in view of U.S. Patent No. 5,396,604 to *DeLano,* and Claims 24 and 30 are rejected under 35 U.S.C. § 103(a) as unpatentable over *Chen* in view of U.S. Patent No. 5,931,957 to *Konigsburg.* Those rejections are respectfully traversed, and favorable reconsideration of the claims is requested.

Applicant respectfully submits that exemplary Claim 18 is not rendered unpatentable by *Chen,* whether considered individually or in combination with the other references of record, because the references of record do not teach or suggest the individual features (or combination of features) recited in the claims as amended herein. For example, *Chen* and the other references of record do not teach or suggest:

> in response to fetching said instruction sequence for execution and prior to execution of said load instruction, instruction processing circuitry detecting said load instruction within said fetched instruction sequence and <u>translating said load instruction into separately executable prefetch and register instructions;</u>
> after the translating, the instruction processing circuitry <u>dispatching the preceding instruction and the prefetch and register instructions for execution;</u>
> <u>execution circuitry receiving the dispatched preceding instruction and the prefetch and register instructions</u> from the instruction processing circuitry;
> in response to receiving the dispatched prefetch instruction, <u>the execution circuitry executing at least said prefetch instruction</u> .... (emphasis supplied)

That is, *Chen* (considered alone or in combination with other references) does not teach or suggest the dynamic translation of a load instruction into a prefetch instruction, the dispatch of a prefetch instruction from instruction processing circuitry to execution circuitry, receipt of the dispatched prefetch instruction by the execution circuitry, and execution by the execution circuitry of the prefetch instruction.

Although paragraphs 9(c) and 9(d) of the present Office Action state that *Chen* discloses execution circuitry performing prefetch operations, upon review of *Chen,* Applicant notes that *Chen* does not teach or suggest a <u>prefetch instruction</u> as claimed. Instead, *Chen* teaches use of a reference prediction table (i.e., a prefetch stride prediction cache) to initiate prefetching by transmitting to the memory subsystem a prefetching address generated utilizing a detected stride (*Chen,* p. 612; Figure 2). *Chen* nowhere teaches or suggests an <u>executable prefetch instruction.</u>

Further confirmation of the fact that *Chen* does not teach or suggest an executable prefetch instruction can be found in *Chen's* Figure 4, which illustrates *Chen's* reference prediction table (RPT) in relation to other elements of an exemplary processor. In particular, it should be noted that *Chen's* RPT, which generates the prefetching address, is separate and distinct from *Chen's* execution unit, and that *Chen's* execution unit does not calculate or receive the prefetching address, which is instead transmitted directly from the RPT to the memory subsystem.

Because *Chen* does not teach or suggest the claimed prefetch instruction, *Chen* does not disclose the claimed steps of "translating said load instruction into separately executable prefetch and register instructions," "dispatching the ... prefetch ... instruction[] for execution," "execution circuitry receiving the dispatched ... prefetch ... instruction[] from the instruction processing circuitry," and "the execution circuitry executing at least said prefetch instruction." Consequently, Applicant respectfully submits that exemplary Claim 18, similar Claim 17 and their respective dependent claims are not rendered unpatentable by *Chen*, whether considered alone or in combination with the other references of record.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant respectfully submits that all pending claims are in condition for allowance and respectfully requests such allowance.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM CORPORATION Deposit Account No. **09-0447**.

Respectfully submitted,

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